GMX™ 256K BYTE STATIC RAM BOARD

User's Manual

GIMIX Inc.
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312-927-5510 * TWX 910-221-4055

GIMIX 256K BYTE STATIC RAM BOARD

FEATURES

* FULLY STATIC MEMORY does not require complicated refresh timing or clocks for data retention. Compatible with any DMA technique.

* GUARANTEED 2+ MHz. OPERATION uses high speed (150ns), 8Kx8 static RAMs with no wait states or clock stretching required.

* ADDRESSABLE in configurations to suit a variety of applications. Full 20 bit address decoding for 1M byte systems. Addressing compatible with OS-9™ GMX™ II and III, UniFLEX™, and FLEX™ with GIMIX-VDISK.

* LOW POWER RAM requires less than 350 ma. typical at 8V, for 256K Bytes. A Megabyte (4 boards) requires less than 1.5 Amps.

* NiCad BATTERY BACKUP for power-off data retention up to 300 Hrs. with a fully charged battery. (optional)

* LOW BUS VOLTAGE DETECTION inhibits memory access during power-up and power-down to prevent false writes to memory. (batt. vers.)

* WRITE-PROTECTABLE for PROM/ROM simulation and software debugging.

CONTENTS

***** NOTE *****

This manual covers both the battery backup and non-battery versions of the GIMIX 256K STATIC RAM BOARD. Except for the information on the battery backup feature the information applies to both versions. The battery and certain other components shown in the schematic are not present in the non-battery version.

***** CAUTION *****

The battery backup versions of the board is particularly subject to damage from improper handling. See the "CAUTION" notices on pages 1 and 5.

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INTRODUCTION

The GIMIX 256K STATIC RAM BOARD provides up to a quarter-megabyte of read/write memory on a single SS-50 board. Only four boards are required for a full megabyte of RAM; allowing more room in the mainframe for I/O and other peripherals. The board consumes less power that previous designs; which helps the system run cooler and extends the capabilities of the power supply. Using fast, 8Kx8 static RAMs and high-speed logic insures reliable performance in 2MHz+ systems.

SECTION 1: HARDWARE CONFIGURATION OPTIONS

There are several hardware jumper options which must be configured before the board is used. These jumpers determine the address of the memory and enable the write-protect and battery backup (optional) features. This section describes each of the option jumpers.

1-1: Bank Size Select Jumper (JA-1)

Since the board can occupy 256K of address space, it spans four "banks" of memory (the 1 Mbyte address space is divided into 16 banks of 64K each by the extended address lines A16-A19). In some system configurations, the upper 4K or 8K of some or all of the banks must be left open for the operating system and cannot contain RAM. This jumper allows parts of certain banks to be disabled. Figures A through F of the Jumper Options Drawing on page 6 show the layout of the jumper and the available options. See the section on addressing for more information.

1-2: Battery ON/OFF Jumper (JA-2) [battery backup version only]

This jumper enables or disables the battery backup feature on boards purchased with this option. Normally the jumper should be configured as shown in figure G of the Jumper Options Drawing on page 6 (battery ON). In this position the contents of the memory will be retained even when the system power is removed. When the jumper is in the "OFF" position (Fig. H) the battery is disconnected from the memory array.

***** CAUTION *****

Use caution when handling boards that have the battery backup installed. Parts of the circuit are "live" even when the board is removed from the system and the battery jumper is in the OFF position. DO NOT place the board on a conductive surface or cause shorts between the conductors on the PC board, as damage to the board and components may result. The battery jumper MUST be in the OFF position when removing ICs from the board or performing other service.

1-3: Write-protect Option Jumper (JA-3)

This jumper gives the user the option of write-protecting part or all of the memory on the board. Normally, with no jumpers installed at JA-3, the board operates as read/write memory. If jumpers are installed or the pins connected together in some other manner, the lower 128K, the upper 128K, or the entire board can be write-protected. Data can be read as always but the board will ignore all writes to the protected section(s). See figures I, J, and K of the Jumper Options Drawing on page 6.

The write-protect option can be enabled by using jumper blocks (as used on the other jumpers). If this feature is used often the user may wish to install a remotely mounted switch (user supplied), connected to the pins of JA-3. If installing a switch for this purpose, be sure it is rated for low current (dry) circuit use and keep wire lengths to a minimum.

1-4: Reserved Jumper (JA-4)

This jumper is reserved for future applications.

1-5: Decoding Configuration Option Jumper (JA-5)

The board is normally supplied with the standard 64K bank decoding option installed (4 banks of 64K each), and this jumper should be configured for 64K decoding as shown in figure N of the Jumper Options Drawings. A decoding option, providing 8 banks of 32K each, is available for special applications. This option requires replacement of the address decoder (U-39). Contact GIMIX for more information.

1-6: Base Address Select Jumper (JA-6)

This jumper selects the base address of the entire board. When using 64K pages (standard), the base address can be any one of four 256K boundaries: $00000, $40000, $80000, or $C0000. The jumper configurations are shown in figures P, Q, R, and S of the Jumper Options drawings on page 6. See the section on addressing for more information.

SECTION 2: ADDRESSING

The board can be addressed to occupy all or part of four consecutive 64K banks, beginning on one of four possible 256K boundaries. To correctly configure the board both the base address and the size of the four banks must be determined and the jumpers (JA-1 and JA-6) set appropriately. Please note that all address references are five digit numbers, with the first digit representing the extended (bank) address.

2-1: Base Address Selection

The base address of the board can be any one of four 256K boundaries in the 1M byte address space ($00000, $40000, $80000, or $C0000). The base address is selected by the configuration of the jumpers at jumper area JA-6. In systems that have only one memory board, its base address MUST be $00000 (Fig. P). This is necessary to meet the operating system's bank 0 memory requirements. If additional boards are installed, they may start at any of the remaining base addresses. Normally, the second board would be addressed at $40000, the third at $80000, and the fourth at $C0000. Each board must have a unique base address.

2-2: Bank Size Selection

The board occupies four consecutive 64K banks of the address space, starting at the base address of the board. For example, a board set to a base address of $00000, occupies banks $0, $1, $2, and $3. The board can be configured so that the entire 64K of each bank is occupied, or so that the upper 4 or 8K of one or all four sections is disabled. In some systems these areas MUST be disabled to prevent conflicts with the operating system PROMs. The following paragraphs describe each of these options. Note: figure references refer to the Jumper Options Drawings on page 6.

FOUR 56K BANKS (Fig. B): When this option is selected, the upper 8K ($xE000-$xFFFF) of all four banks is disabled. This option is used for all boards in OS-9 GMX II systems with unmodified CPU boards.

FOUR 64K BANKS (Fig. C): When this option is selected no memory is disabled. The board occupies the entire 64K of each of the four banks. This option can be used for the first three boards ($00000, $40000, and $80000) in GMX III systems (OS-9 GMX III) and in OS-9 GMX II systems where the CPU board has been modified to support 64K banks.

THREE 64K BANKS and ONE 56K BANK (Fig. D): When this option is selected only the upper 8K ($xE000-$xFFFF) of the last bank (highest address) is disabled. This option is used for the fourth board (base address $C0000) in GMX III systems (OS-9 GMX III) and in OS-9 GMX II systems where the CPU board has been modified to support 64K banks.

FOUR 60K BANKS (Fig. E): When this option is selected, the upper 4K ($xF000-$xFFFF) of all four banks is disabled. This option is used for special applications.

THREE 64K BANKS and ONE 60K BANK (Fig. F): When this option is selected, only the upper 4K ($xF000-$xFFFF) of the last bank (highest address) is disabled. This option is used for special applications.

2-3: Standard Addressing for GIMIX Systems

The following tables show the standard address jumper (JA-1 and JA-6) configurations for GIMIX systems using from one to four 256K RAM boards.

OS-9 GMX III systems and OS-9 GMX II with modified CPU boards

Board	JA-1 Fig.	JA-6 Fig.	MEMORY ADDRESSES 1	2	3	4
1st	C	P	$00000-$0FFFF	$10000-$1FFFF	$20000-$2FFFF	$30000-$3FFFF
2nd	C	Q	$40000-$4FFFF	$50000-$5FFFF	$60000-$6FFFF	$70000-$7FFFF
3rd	C	R	$80000-$8FFFF	$90000-$9FFFF	$A0000-$AFFFF	$B0000-$BFFFF
4th	D	S	$C0000-$CFFFF	$D0000-$DFFFF	$E0000-$EFFFF	$F0000-$FDFFF

OS-9 GMX II systems with unmodified CPU boards

Board	JA-1 Fig.	JA-6 Fig.	MEMORY ADDRESSES 1	2	3	4
1st	B	P	$00000-$0DFFF	$10000-$1DFFF	$20000-$2DFFF	$30000-$3DFFF
2nd	B	Q	$40000-$4DFFF	$50000-$5DFFF	$60000-$6DFFF	$70000-$7DFFF
3rd	B	R	$80000-$8DFFF	$90000-$9DFFF	$A0000-$ADFFF	$B0000-$BDFFF
4th	B	S	$C0000-$CDFFF	$D0000-$DDFFF	$E0000-$EDFFF	$F0000-$FDFFF

SECTION 3: BATTERY BACKUP

The on-board Nickel-cadmium battery provides the power required to retain data in the memory when system power is removed. Data remains intact for a minimum of 300 hours with a fully charged battery. The battery is trickle charged whenever system power is applied to the board and the battery ON/OFF jumper is in the ON position. The transition between system and battery power is automatic. An adjustable unsafe voltage circuit monitors the +8V bus and inhibits memory accesses whenever the bus voltage falls below a preset safe level. This prevents false writes to the memory when the system bus is in an undefined state during power-up and down.

***** CAUTION *****

When the battery ON/OFF jumper (JA-2) is in the ON position, power is applied to the memory array at all times, even when the board is removed from the system. Before removing or installing parts the battery ON/OFF jumper must be placed in the OFF position to prevent possible damage to the parts. Use caution when handling the board to prevent shorting the battery terminals together or to other parts of the circuit as damage to the battery/board may occur.

3-1: Voltage Threshold Adjustment

The voltage at which the unsafe voltage detector activates is determined by the setting of trimmer resistor R7. This adjustment is factory set at a voltage just above the point where the on-board voltage regulator falls out of regulation, approximately 7 volts, and should not need readjustment under normal circumstances.

***** NOTE *****

In certain non-GIMIX systems the bus voltage may be too low to allow proper operation of the board. These systems will require modifications to their power supplies to provide sufficient voltage. The nominal +8V bus voltage should be somewhat above the setting of the unsafe voltage threshold to provide for normal voltage fluctuations.

Appendix A
Special Address Configuration for 32/24K banks

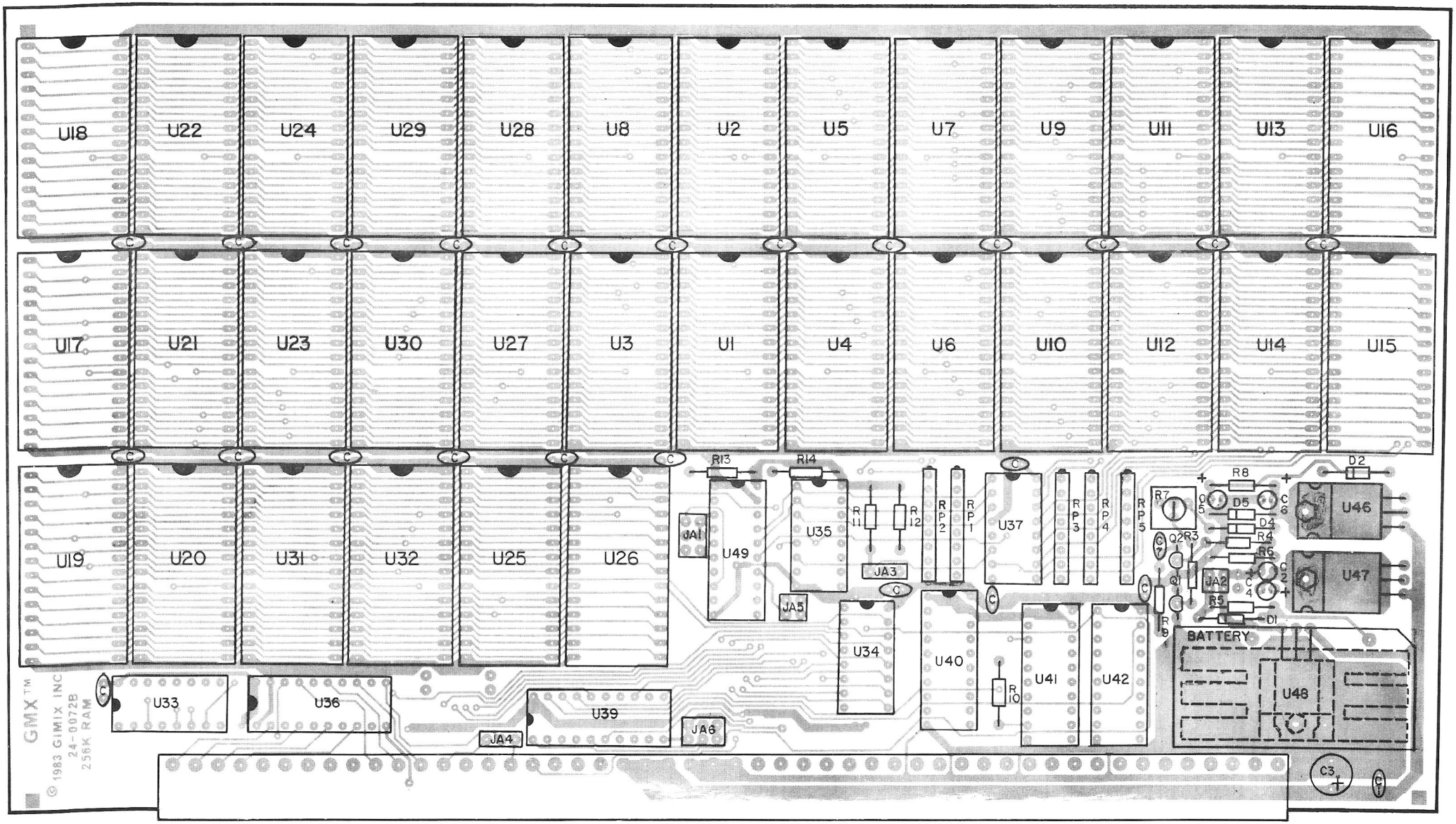
With decoding IC(U39) PN 12E1

In some applications it may be advantageous to address the GIMIX 256K Static RAM board in 32K pages rather than the standard 64K pages. This can only be accomplished if the board is equipped with a special version of the address decoder (IC U-39). When the special 32K decoder (part no. 12E1) is installed the following table must be used to select the board addressing.

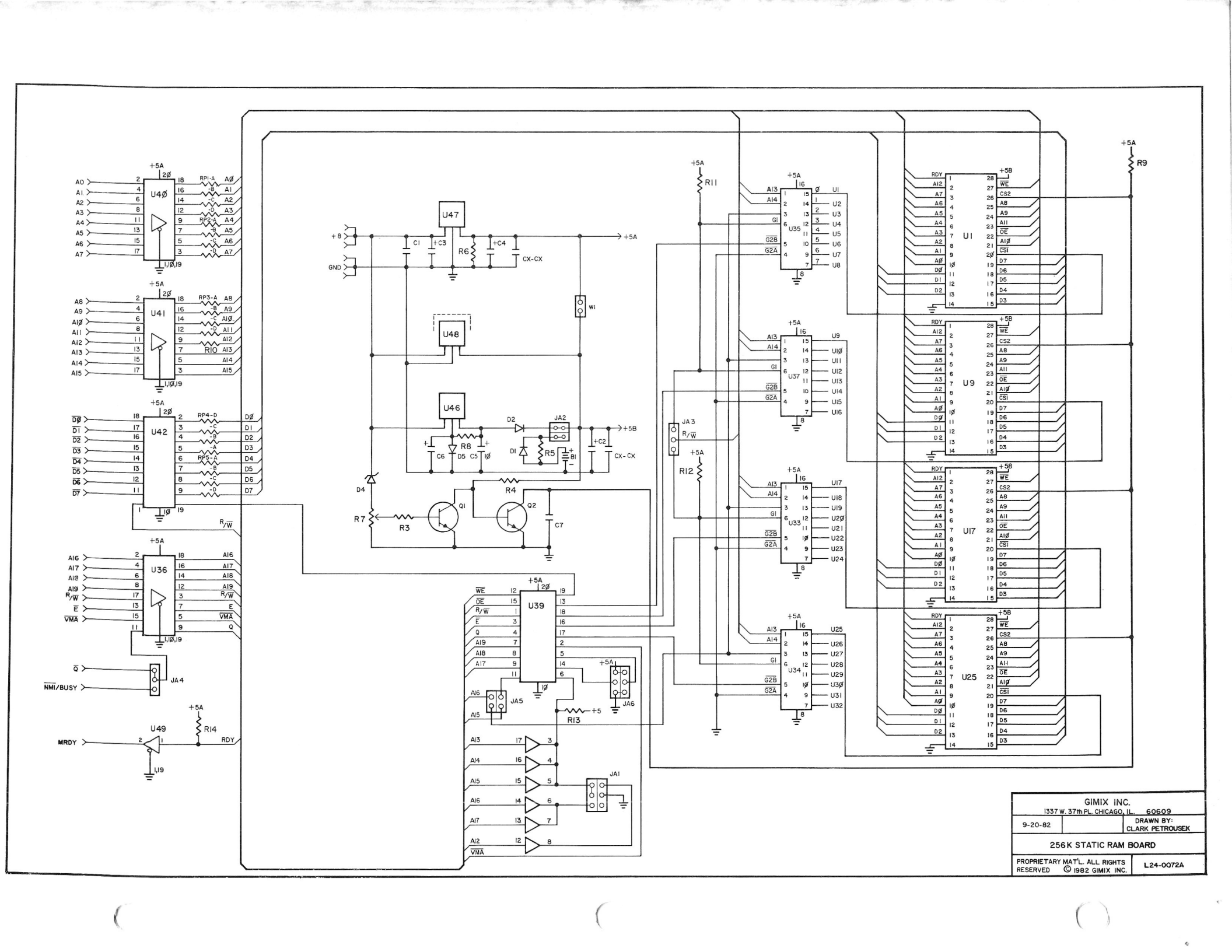
Board	JA-1 Fig.	JA-5 Fig.	JA-6 Fig.	MEMORY ADDRESSES 1	2	3	4
1st	B	0	P	$00000-$07FFF	$20000-$27FFF	$40000-$47FFF	$60000-$67FFF
	Lower 32K Banks $0-$7			$10000-$17FFF	$30000-$37FFF	$50000-$57FFF	$70000-$77FFF
2nd	B	0	Q	$80000-$87FFF	$A0000-$A7FFF	$C0000-$C7FFF	$E0000-$E7FFF
	Lower 32K Banks $8-$F			$90000-$97FFF	$B0000-$B7FFF	$D0000-$D7FFF	$F0000-$F7FFF
3rd	B	0	R	$08000-$0DFFF	$28000-$2DFFF	$48000-$4DFFF	$68000-$6DFFF
	Upper 32K † Banks $0-$7			$18000-$1DFFF	$38000-$3DFFF	$58000-$5DFFF	$78000-$7DFFF
4th	B	0	S	$88000-$8DFFF	$A8000-$ADFFF	$C8000-$CDFFF	$E8000-$EDFFF
	Upper 32K † Banks $8-$F			$98000-$9DFFF	$B8000-$BDFFF	$D8000-$DDFFF	$F8000-$FDFFF

† Note: When the upper 32K is selected, only 24K appears in each bank. The upper 8K of each bank is disabled for I/O and system ROM use.

Figure designations in the above table refer to the standard Jumper Options drawing (C24-0072A) in the 256K RAM manual.



COMPONENT LAYOUT



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JA-1

FIG. A

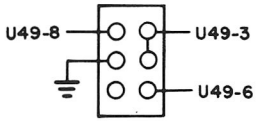
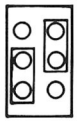
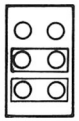


FIG. B



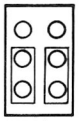
4x56K BANKS

FIG. C



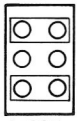
4x64K BANKS

FIG. D



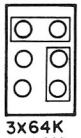
3x64K 1x56K BANKS

FIG. E



4x60K BANKS

FIG. F



3x64K 1x60K BANKS

BANK SIZE SELECT

JA-2

FIG. G

BATTERY ON

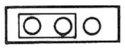
FIG. H

BATTERY OFF

BATTERY ON/OFF JUMPER

JA-3

FIG. I

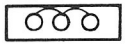


LOWER 2 BANKS PROTECTED

FIG. J

UPPER 2 BANKS PROTECTED

FIG. K



ALL BANKS PROTECTED

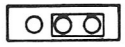
WRITE PROTECT OPTION

JA-4

FIG. L

STANDARD

FIG. M



SPECIAL

RESERVED FOR FUTURE USE

JA-5

FIG. N

STANDARD (64K VERSION)

FIG. O

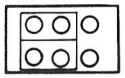
OPTIONAL * (32K VERSION)

DECODING CONFIGURATION OPTION

* NOTE: THE 32K OPTION, REQIRES A DIFFERENT DECODING I.C. (U-39).

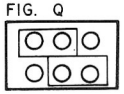
JA-6

FIG. P



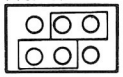
BANKS $0-$3

FIG. Q



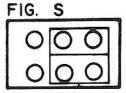
BANKS $4-$7

FIG. R



BANKS $8-$B

FIG. S



BANKS $C-$F

BANK ADDRESS SELECT

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256K STATIC RAM BOARD JUMPER OPTIONS

C24-0072A